

sub
I1
a transistor having an enable terminal, an input terminal, and an output terminal,
said input terminal coupled to receive binary signals from the first circuit that vary
between first and second preselected voltage levels, and said output terminal coupled to
deliver binary signals to a second circuit that vary between the first preselected voltage
level and a third preselected voltage level;

cont'd
a capacitor coupled across said input and output terminals of said transistor; and
a resistive element having a first end portion coupled to the enable terminal of
said transistor and a second end portion coupled to a voltage supply to bias the transistor
continuously on, the resistive element cooperating with a parasitic capacitor defined by
said transistor to increase the voltage applied to the enable terminal during a transition
from the first to the second preselected voltage level at the input terminal.

sub
I2
8. (Fourth Amendment) An apparatus for converting first digital signals that vary
between a first and second preselected voltage levels to second digital signals that vary
between the first and a third preselected voltage level, comprising:

a first circuit;

a pass gate transistor having a gate, source, and drain, said drain coupled to said
first circuit to receive said first signals, said source coupled to a second circuit to deliver
said second signals, said gate coupled to a voltage supply;

a capacitor coupled across said source and drain of said pass gate transistor; and
a pump coupled to the gate of said pass gate transistor, said pump being
configured to increase the voltage level applied to said gate during a transition from the
first to the second preselected voltage levels.

sub
I 3

13. (Fourth Amendment) An apparatus for converting an input signal that varies between first and second preselected voltage levels to an output signal that varies between the first preselected voltage level and a third preselected voltage level, comprising:

a first circuit;

a pass gate transistor having a gate, source, and drain, said drain coupled to said first circuit to receive said input signal, said source coupled to a second circuit to deliver said output signal, said gate being coupled to a voltage supply;

a capacitor coupled across said source and drain of said pass gate transistor; and

means for increasing the voltage level applied to said gate during a transition of the input signal from the first to the second preselected voltage level.

sub
I 4

17. (Second Amendment) A buffer circuit, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to a first circuit to receive a first digital signal that varies between first and second voltage levels;

a first voltage supply coupled to the gate of said pass gate transistor to bias the transistor continuously on;

a capacitor coupled across the source and drain of said pass gate transistor;

an inverter having an input terminal and an output terminal, said input terminal coupled to the source of said pass gate transistor to receive a second digital signal that varies between the first voltage level and a third voltage level;